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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/878,554	06/11/2001	Xinghao Chen	FIS920010060US1	5168

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EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 04/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/878,554	CHEN ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,6 and 8-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,6 and 8-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claim*** have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claims 2, 6 and 8-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Song et al. (Song, O.; Menon, P.R.; Parallel pattern fault simulation based on stem faults in combinational circuits, Proceedings International Test Conference, 10-14 Sept. 1990, Pages:706 – 711) [hereafter referred to as Song] in view of Maruyama; Daisuke (US 6205567 B1).

35 U.S.C. 103(a) rejection of claim 2.

Song teaches a) performing a good machine simulation of the IC with the test to obtain values of each internal node of the IC (the last few line in column 2 on page 707 of Song teaches True value simulation for determining fault-free values on all lines of the circuit; Note: true value simulation is a good machine simulation and fault-free values of lines are values also values associated with the node vertices to which the lines led into since input lines to a node vertex uniquely define the node and the line value is also a node vertex value for a particular input to the node vertex); b) based on the good machine simulation, identifying potential faults to be tested by the test by backtracing, in a single detection pass, starting at each observable node, said backtracing being based on outputs of stems, the outputs stems being obtained from said good machine simulation said backtracing being limited to paths along which a faulty value has a possibility of propagating to said observable node (Procedure 1 at the bottom of column 2 on page 707 and the top of column 1 on page 708 of Song is an algorithm for identifying potential faults to be tested by the test by backtracing, in a single detection pass for every set of vectors, starting at each observable node PO, said backtracing being based on outputs of stems, the outputs stems being obtained from said good machine simulation; the last paragraph in column 2 on page 708 of Song teaches said backtracing being limited to paths along which a faulty value has a possibility of propagating to said observable node since any undetectable fault is eliminated from paths); c) with the test, performing the fault simulation on the potential faults to be

tested (Procedure 1 at the bottom of column 2 on page 707 and the top of column 1 on page 708 of Song is an algorithm for performing the fault simulation on the potential faults to be tested); and d) repeating a) through c) for additional tests of the plurality of tests (Procedure 1 at the bottom of column 2 on page 707 and the top of column 1 on page 708 of Song is repeatedly performed for each set of test patterns).

However Song does not explicitly teach the specific use of a good machine simulation on the IC having logic gates and memory elements.

Maruyama, in an analogous art, teaches use of a good machine simulation on the IC having logic gates and memory elements (col. 12, lines 11-13 in Maruyama).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Song with the teachings of Maruyama by including use of a good machine simulation on the IC having logic gates and memory elements. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a good machine simulation on the IC having logic gates and memory elements would have provided a required means for determining whether a fault can be detected (col. 1, lines 30-36 in Maruyama).

35 U.S.C. 103(a) rejection of claims 6.

See last paragraph in column 2 on page 706 of Maruyama.

35 U.S.C. 103(a) rejection of claims 8-10.

Song teaches a) performing a good machine simulation of the IC with the test to obtain values of each internal node of the IC (the last few line in column 2 on page 707 of Song teaches True value simulation for determining fault-free values on all lines of the circuit; Note: true value simulation is a good machine simulation and fault-free values of lines are values also values associated with the node vertices to which the lines led into since input lines to a node vertex uniquely define the node and the line value is also a node vertex value for a particular input to the node vertex); b) based on the good machine simulation, identifying potential faults to be tested by the test by backtracing, in a single detection pass, starting at each observable node, said backtracing being based on outputs of stems, the outputs stems being obtained from said good machine simulation said backtracing being limited to paths along which a faulty value has a possibility of propagating to said observable node (Procedure 1 at the bottom of column 2 on page 707 and the top of column 1 on page 708 of Song is an algorithm for identifying potential faults to be tested by the test by backtracing, in a single detection pass for every set of vectors, starting at each observable node PO, said backtracing being based on outputs of stems, the outputs stems being obtained from said good machine simulation; the last paragraph in column 2 on page 708 of Song teaches said backtracing being limited to paths along which a faulty value has a possibility of propagating to said observable node since any undetectable fault is eliminated from paths); c) with the test, performing the fault simulation on the potential faults to be tested (Procedure 1 at the bottom of column 2 on page 707 and the top of column 1 on page 708 of Song is an algorithm for performing the fault simulation on the potential

faults to be tested); and d) repeating a) through c) for additional tests of the plurality of tests (Procedure 1 at the bottom of column 2 on page 707 and the top of column 1 on page 708 of Song is repeatedly performed for each set of test patterns). Note: undetectable faults are faults that are blocked from being observed by the test and limiting backtracing to paths along which a faulty value has a possibility of propagating by eliminating undetectable faults from paths is a means for blocking testing of undetectable faults.

However Song does not explicitly teach the specific use of a good machine simulation on the IC having logic gates and memory elements.

Maruyama, in an analogous art, teaches use of a good machine simulation on the IC having logic gates and memory elements (col. 12, lines 11-13 in Maruyama).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Song with the teachings of Maruyama by including use of a good machine simulation on the IC having logic gates and memory elements. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a good machine simulation on the IC having logic gates and memory elements would have provided a required means for determining whether a fault can be detected (col. 1, lines 30-36 in Maruyama).

35 U.S.C. 103(a) rejection of claims 11-13.

The first paragraph at the top of column 1 on page 708 of Song teaches that backtracing take place form stems where a stem fault is detected.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JOSEPH TORRES
PRIMARY EXAMINER

Joseph D. Torres, PhD
Primary Examiner
Art Unit 2133